AMENDMENTS TO THE CLAIMS

In accordance with the PTO's amendment format, a detailed listing of all claims has been provided. A status identifier is provided for each claim in parentheses following each claim number.

In the Claims:

Claims 1-13, 15-25 were previously pending.

Please amend claims 1, 6, and 11.

Claim 14 is previously canceled.

Please cancel claims 21-25.

No new claims are added.

Claims 1-13, 15-20 are currently pending.

Listing of the Claims

1. (Currently Amended) A method for debugging a target computer that utilizes virtual memory paging, the method comprising:

replicating on a host computer an address translation table of the target computer, wherein the address translation table establishes on the host computer correspondences between physical memory addresses and virtual memory addresses that existed on the target computer;

transferring physical memory data from the target computer to the [[a]] host computer; and

replicating virtual memory data from the physical memory data on the host computer, wherein the virtual memory data on the host computer is identical to virtual memory data on the target computer.

2. (Original) The method as recited in claim 1, further comprising debugging a fault on the target computer by analyzing replicated data on the host computer.

3. (Original) The method as recited in claim 1, further comprising caching the replicated data in memory on the host computer.

4. (Original) The method as recited in claim 1, wherein the target computer includes an operating system that uses table-driven paged memory management.

5. (Previously Presented) The method as recited in claim 1, wherein:

the target computer includes a processor that has halted execution; and

the virtual memory data is located in physical memory of the target computer.

6. (Currently Amended) A host computing system, comprising:

a processor;

memory;

means for establishing a connection between the memory and memory of a target computer;

a data retrieval component configured to transfer address table data from memory of the target computer to the memory;

an address translation component configured to replicate virtual memory addresses from the address table data in the memory; and

wherein the virtual memory data in the host computing system are identical to virtual memory data of the target computer for debugging the target computer when a CPU of the target computer is halted.

7. (Original) The host computing system as recited in claim 6, further comprising cache memory configured to store the replicated virtual memory addresses.

8. (Original) The host computing system as recited in claim 6, wherein the host-side address translation component is further configured to validate the replicated virtual memory addresses.

9. (Original) The host computing system as recited in claim 6, further comprising a memory management verifier that verifies that a processor of the target computing system has memory management enabled.

10. (Original) The host computing system as recited in claim 6, wherein the means for establishing a connection between the memory and memory of a target computer comprises hardware-assisted debug probes.

11. (Currently Amended) A method, comprising:

accessing address tables from physical memory of a target computer system by reading the target memory directly through an application program interface;

replicating the address tables on a host computing system; and

using data contained in the address tables to derive virtual address data that was used on the target computer system, wherein the virtual address data on the host computer system are identical to virtual address data on the target computer system.

12. (Original) The method as recited in claim 11, further comprising storing the address tables in memory on the host computer system.

13. (Original) The method as recited in claim 11, further comprising caching the virtual address data on the host computer system.

14. (Canceled)

15. (Original) The method as recited in claim 11, further comprising determining if memory management of a target computer system processor is enabled.

16. (Original) The method as recited in claim 11, further comprising performing the method only if memory management of a target computer system processor is enabled.

17. (Original) The method as recited in claim 11, wherein the accessing further comprises:

locating the address tables in physical memory of the target computer system; and

reading the address tables from the target computer.

18. (Original) The method as recited in claim 11, further comprising validating the virtual address data to ensure it is identical to the virtual address data stored on the target computer system.

19. (Original) The method as recited in claim 11, further comprising debugging a fault that occurred on the target computer by analyzing the virtual address data on the host computer system.

20. (Original) A computer-readable medium containing processor-executable instructions that, when executed on a processor, perform the method of claim 11.

21-25. (Canceled)